UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/088,674	06/02/1998	DANIEL J. MORGAN	TI-25995	2025

23494   7590   01/16/2007
TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER
NGUYEN, KEVIN M

ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
2 MONTHS	01/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

PTOL-90A (Rev. 10/06)

MAILED

JAN 1 6 2007

Technology Center 2600

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Application Number: 09/088,674
Filing Date: June 02, 1998
Appellant(s): MORGAN ET AL.

MORGAN ET AL.
<u>For Appellant</u>

EXAMINER'S ANSWER

This is in response to the appeal brief filed 20 October 2006 appealing from the Office action mailed 15 November 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,222,515	YAMAGUCHI ET AL.	4-2001
5,731,802	ARAS ET AL.	3-1998

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form

the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1.   Claims 1-3, 5-8 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated

by Yamaguchi et al (US 6,222,515).

2.   As to claim 1, Yamaguchi et al teach a system of displaying digital video data

associated with a method comprising: a first pixel value defined by [(3V) is mean

effective voltage], see fig. 7B.

Yamaguchi et al further inherently teach a first predetermined amount "-1"

[defined by an area hatching from 3V to 2V at the first field] to form a first offset pixel

value [defined by 2V at the first field], and displaying said first offset pixel during a first

frame period [2V at the first filed, see fig. 7B];

Yamaguchi et al further inherently teach the opposite of said predetermined

amount "+1" [defined by an area hatching from 3V to 4V at the first field] to form a

second offset pixel value [defined by 4V at a second field], and displaying said second

offset pixel during a second frame period [4V at the second filed, see fig. 7B];

Yamaguchi et al further teach the average of said displayed first offset pixel value [2V at the first filed] and said second offset pixel value [4V at the first filed] is said first pixel value (3V) [(3V) is mean effective voltage which is shown by area hatching in figure 7B" (see fig. 7B, col. 8, lines 11-27)].

3.   As to claim 6, Yamaguchi et al inherently teach a logic circuit defined by means for offsetting inherently a first predetermined amount "-1" [defined by an area hatching from 3V to 2V at the first field] to form a first offset pixel value [defined by 2V at the first field]

Yamaguchi et al further inherently teach a logic circuit defined by means for offsetting inherently by the opposite of said predetermined amount "+1" [defined by an area hatching from 3V to 4V at the second field] to form a second offset pixel value [defined by 4V at a second field].

Yamaguchi et al further teach a display panel 19 (display means, fig. 1B) which displays said first offset pixel during a first frame period [2V at the first filed, see fig. 7B], and displays said second offset pixel during a second frame period [4V at the second filed, see fig. 7B].

Yamaguchi et al further teach the average of said displayed first offset pixel value [2V at the first filed] and said second offset pixel value [4V at the first filed] is said first pixel value (3V) [(3V) is mean effective voltage which is shown by hatching in figure 7B" (see fig. 7B, col. 8, lines 11-27).

4.   As to claims 2 and 7, Yamaguchi et al inherently teach said first predetermined amount "-1" [defined by 2V-3V at the first field], said predetermined amount "+1"

[defined by 4V-3V at the first field]. Thus, said first predetermined amount "-1" is selectively as a function of (X-3).

5.   As to claims 3 and 8, Yamaguchi et al teach said first offset pixel value 2V is less than said first pixel value (3V) as a function (X-3) of the spatial location ["-1" defined the spatial location] that [(3V) is mean effective voltage] defined to be displayed.

6.   As to claims 5 and 10, Yamaguchi et al show the fig. 7 including the first field are consecutive the second field.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7.   Claims 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al in view of Aras et al (US 5,731,802).

8.   As to claims 4 and 9, Yamaguchi et al teach all of the claimed limitations of claims 1 and 6, except for display uses a plurality of weighted bit-plane, wherein said first pixel values close to a bit transition of said bit-planes are offset during said display frame and said second frame.

However, Aras et al teach the number of rows multiplied by the number of bits in grayscale weighting is equal to the number of update event per frame or write cycle per frame (fig. 4, col. 5, lines 32-34). Rows 0, 1 and 2 are loaded with the data for the 0th, 3rd and 2nd weight bits, respectively. The number of data transitions per clock cycle

during the next clock cycle of the data in rows 1 and 2 changes such that rows 1 and 2 are loaded with the data for its 0th and 3rd weight bits, respectively (col. 6, lines 26-37).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Yamaguchi et al's field (frame, fig. 7) including rows 0, 1 and 2 are loaded with the data for the 0th, 3rd and 2nd weight bits, respectively. The number of data transitions per clock cycle during the next clock cycle of the data in rows 1 and 2 changes such that rows 1 and 2 are loaded with the data for its 0th and 3rd weight bits, respectively, in view of the teaching in the Aras et al's reference, because this would provide gray scale using a weighted PWM scheme which does not flicker and provides a reduced bandwidth requirement for the associated control circuitry and data bus as taught by Aras et al (col. 3, lines 41-44).

(10) Response to Argument

A.   Ground of 102 rejection:

MPEP section 2131 paragraphs II and III explain of each circumstance.

Extra References or Other Evidence Can Be Used to Show Meaning of a Term Used in the Primary Reference. Extrinsic evidence may be used to explain but not expand the meaning of terms and phrases used in the reference relied upon as anticipatory of the claimed subject matter. In re Baxter Travenol Labs., 952 F.2d 388, 21 USPQ2d 1281 (Fed. Cir. 1991).

Extra Reference or Evidence Can Be Used To Show an Inherent Characteristic of the Thing Taught by the Primary Reference "To serve as an anticipation when the reference is silent about the asserted inherent

characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). Note that as long as there is evidence of record establishing inherency, failure of those skilled in the art to contemporaneously recognize an inherent property, function or ingredient of a prior art reference does not preclude a finding of anticipation. Atlas Powder Co. v. IRECO, Inc., 190 F.3d 1342, 1349, 51 USPQ2d 1943, 1948 (Fed. Cir. 1999). This finding of inherency was not defeated by the fact that one of the references taught away from air entrapment or purposeful aeration.). See also In re King, 801 F.2d 1324, 1327, 231 USPQ 136, 139 (Fed. Cir. 1986); Titanium Metals Corp. v. Banner, 778 F.2d 775, 782, 227 USPQ 773, 778 (Fed. Cir. 1985). See MPEP § 2112- § 2112.02 for case law on inherency. Also note that the critical date of extrinsic evidence showing a universal fact need not antedate the filing date. See MPEP §2124.

Since only alleged distinction between appellant's claims and reference is recited in functional language, it is incumbent upon appellants, when challenged, to show that device disclosed by reference does not actually possess such characteristics. See In re Ludtke, 169 USPQ 563 (CCPA) 1971). The burden on appellant to rebut an inherency rejection applied to product and process claims. See In re Best, 195 USPQ 430, 433 (CCPA 1977).

The case law stated that "Drawing as a Reference", "Things clearly shown in reference patent drawing qualify as prior art features, even though unexplained by the specification". see In re Mraz, 173 USPQ 25 (CCPA 1972). "A claimed invention may be anticipated or rendered obvious by a drawing in a reference, whether the drawing disclosure by accidental or intentional. However, a drawing is only available as a reference for what it would teach one skilled in the art who did not have the benefit of appellant's disclosure". See In re Meng, 181 USPQ 94, 97 (CCPA 1974). "Absent of any written description in the reference specification of quantitative values, arguments based on measurement of a drawing are of little value in proving anticipation of a particular length". See In re Wright, 193 USPQ 332, 335 (CCPA 1977).

Appellant argues with respect to claim 1, Yamaguchi et al (Yamaguchi) fails to teach "offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value." In response, the examiner respectfully disagrees. As stated *supra* with respect to claim 1, the examiner finds that with a person of ordinary skills in the mathematic and figure 7B of Yamaguchi expressly shows a first pixel value defined by (3V) is mean effective voltage. The at least one Fig. 7B of Yamaguchi further shows a first predetermined amount "-1" defined by an area

hatching from 3V to 2V at the first field to form a first offset pixel value defined by 2V at

the first field, and displaying said first offset pixel during a first frame period 2V at the

first filed. The at least one Fig. 7B of Yamaguchi further shows the opposite of said

predetermined amount "+1" defined by an area hatching from 3V to 4V at the first field

to form a second offset pixel value defined by 4V at a second field, and displaying said

second offset pixel during a second frame period 4V at the second filed. The at least

one Fig. 7B of Yamaguchi further shows the average of said displayed first offset pixel

value 2V at the first filed and said second offset pixel value 4V at the first filed is said

first pixel value (3V) is mean effective voltage which is shown by area hatching in figure

7B (see col. 8, lines 11-27). Furthermore, the gray scale voltage of the teaching of

Yamaguchi is value associated with a pixel in a digital image, representing the

brightness of the original scene in the vicinity of the point represented by the pixel.

Synonyms: gray shade; gray tone; gray level.

Appellant argues with respect to claim 6, Yamaguchi fails to teach "a logic circuit

offsetting a first pixel value a first predetermined amount to form a first offset pixel value,

said logic circuit also offsetting said first said pixel value by the opposite of said first

predetermined amount to form a second offset pixel value." In response, the examiner

respectfully disagrees. As stated *infra* with respect to claim 6, the examiner finds that

Yamaguchi inherently teaches the average circuit corresponding to the logic circuit that

performs the corresponding function that is similar to those of claim 1, though in

apparatus form, therefore the rejection of claim 6, will be treated using the same

rationale as recited in claim 1.

Appellant argues with respect to claims 2 and 7, Yamaguchi fails to teach

"wherein the value of said first predetermined amount is selected as a function of said

first pixel value." In response, the examiner respectfully disagrees. As stated *supra* with

respect to claims 2 and 7, the examiner finds that with a person of ordinary skills in the

mathematic and Yamaguchi inherently teaches said first predetermined amount "-1"

defined by 2V-3V at the first field, said predetermined amount "+1" defined by 4V-3V at

the first field. Thus, said first predetermined amount "-1" and "+1" are selectively as a

function of (X-3), where X is equal to 2V, and X is equal to 4V.

Appellant argues with respect to claims 3 and 8, Yamaguchi fails to teach

"wherein said first offset pixel value is greater than or less than said first pixel value as a

function of the spatial location that said first pixel value is to be displayed." In response,

the examiner respectfully disagrees. As stated *supra* with respect to claims 3 and 8, the

examiner finds that Yamaguchi inherently teaches said first offset pixel value 2V is less

than said first pixel value (3V) as a function (X-3) of the spatial location "-1" defined the

spatial location that (3V) is mean effective voltage defined to be displayed. Therefore,

the first dimension "-1" to concentrate on is the spatial location as claimed.

B.   Ground of 103 rejection:

A prima facie case of obvious is established when the teachings from the prior art

itself would appear to have suggested the claimed subject matter to a person of

ordinary skill in the art. Once such a case is established, it is incumbent upon appellant

to go forward with objective evidence of unobviousness. See In re Fielder, 471 F.2d

640, 176 USPQ 300 (CCPA 1973). See In re Palmer, 172 USPQ 126 (CCPA 1971).

See In re Reven, 156 USPQ 679 (CCPA 1968).

In response to appellant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Appellant argues with respect to claims 4 and 9, the combination of Yamaguchi and Aras et al. (Aras) fails to teach "wherein said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame." In response, the examiner respectfully disagrees. As stated supra, the examiner finds that with respect to claims 4 and 9 based on Yamaguchi in view of Aras, Aras further teaches the time-interleaved bit-plane which includes the number of rows multiplied by the number of bits in grayscale weighting is equal to the number of update event per frame or write cycle per frame (fig. 4, col. 5, lines 32-34). Rows 0, 1 and 2 are loaded with the data for the 0th, 3rd and 2nd weight bits, respectively. The number of data transitions per clock cycle during the next clock cycle of the data in rows 1 and 2 changes such that rows 1 and 2 are loaded with the data for its 0th and 3rd weight bits, respectively (col. 6, lines 26-37). Therefore, it would have been obvious to a person of

ordinary skill in the art at the time the invention was made to modify "weight" gray scale level of Yamaguchi to make time-interleaved close to the number of data transitions bit-plane in view of Aras in order to pre-select an optimized bandwidth or organized into a predetermined format to achieve a pseudo-random effect (see abstract of Aras et al.).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Kevin M. Nguyen

Kevin M. Nguyen

Patent Examiner

Conferees:

Richard Hjerpe

Amr Awad AA

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600